

What is claimed is:

1 I A semiconductor device comprising:
2 external contacts;
3 a metal layer; and
4 a passivation layer being located between the metal layer and the contact and including
5 windows through which the contacts extend to make electrical connections with the metal layer,
6 the windows being selectively size to impart a higher current carrying capability to at least one of
7 the external contacts than to the remaining one or more external contacts.

1 2. The semiconductor device of claim 1, wherein the external contacts comprise
2 solder bumps.

1 3. The semiconductor device of claim 1, further comprising:
2 a power bus in communication with at least one of the external contacts that have a
3 higher current carrying capability.

1 4. The semiconductor device of claim 1, wherein at least one of the external contacts
2 that have a higher current carrying capability is elongated along an axis that generally follows a
3 bus to which the external contact is connected.

1 5. The semiconductor device of claim 1, wherein the metal layer comprises a
2 conductive region in contact with the solder bump, the region being elongated along another axis
3 that is generally aligned with said at least part of the path.

1 6. The semiconductor device of claim 1, wherein the path comprises an
2 approximately straight line and the axis is generally parallel to the straight line.

1 7. The semiconductor device of claim 1, wherein at least one of the windows
2 comprises one of a rectangular window and a hexagonal window.

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1 8. The semiconductor device of claim 1, wherein the windows comprise a first set of
2 at least one window that has a first size and a second set of at least one window that has a
3 significantly larger second size.

1 19. An electrical device comprising:
2 electrical contact pads to receive a supply voltage;
3 a power bus electrically connected to the electrical contact pads; and
4 an interconnection circuit to, for each electrical contact pad, form a redundant connection
5 between the bus and the electrical contact pad.

1 10. The electrical device of claim 9, wherein
2 the electrical device comprises a semiconductor device comprising having multiple
3 process layers, and
4 the interconnection circuit is formed in the same process layer as the power bus.

1 11. The electrical device of claim 9, wherein
2 the electrical device comprises a semiconductor device comprising having multiple
3 process layers, and
4 the interconnection circuit is formed in one of the process layers located between another
5 one of the process layers in which the bus is formed and the electrical contacts.

1 12. The electrical device of claim 9, wherein the interconnection circuit comprises:
2 switches to selectively form the redundant connections.

1 13. The electrical device of claim 9, wherein the device comprises a microprocessor.

*See Attached
Concise*

1 14. A method usable with a semiconductor device, comprising:
2 providing a passivation layer;
3 providing windows in the passivation layer;
4 extending external contacts through the window to make an electrical connection with a
5 metal layer of the semiconductor device; and
selectively sizing the windows to impart a higher current capability to at least one of the
external contacts than to the remaining one or more external contacts.

1 15. The method of claim 14, wherein the external contacts comprise solder bumps.

1 16. The method of claim 14, further comprising:
2 providing a power bus in communication with at least one of the external contacts that
3 have a higher current carrying capability.

1 17. The method of claim 14, wherein the path comprises an approximately straight
2 line and the axis is generally parallel to the straight line.

1 18. The method of claim 14, wherein at least one of the windows comprises one of a
2 rectangular and a hexagonal window.

1 19. The method of claim 14, wherein the windows comprise a first set of at least one
2 window that has a first size and a second set of at least one window that has a significantly larger
3 second size.

1 20. A method usable with a semiconductor device, comprising:
2 electrical connecting external contacts of a semiconductor device to internal buses of the
3 semiconductor device; and
4 establishing redundant connections between the buses and the external contacts.

1 21. The method of claim 20, further comprising:
2 forming the buses in a first process layer; and
3 forming the redundant connections in the same first process layer.

1 22. The method of claim 20, further comprising:
2 forming the buses in a first process layer; and
3 forming the redundant connections in a second process layer different from the first
4 process layer.

1 23. The method of claim 20, further comprising:
2 forming a passivation layer;
3 providing contacts that are exposed for external connections with the semiconductor
4 device on one side of the passivation layer; and
5 forming the redundant connections on said one side.

1 24. The method of claim 23, wherein the forming comprises:
2 depositing a metal layer on said one side; and
3 selectively etching the metal layer to form the redundant connections.